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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/673,507	09/30/2003	Eric J. Strang	231751US6YA	1662

22850 7590 03/05/2010

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EXAMINER	
SAXENA, AKASH	

ART UNIT	PAPER NUMBER
2128	

NOTIFICATION DATE	DELIVERY MODE
03/05/2010	ELECTRONIC

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ERIC J. STRANG

Appeal 2009-007902
Application 10/673,507
Technology Center 2100

Decided: March 3, 2010

Before JAMES D. THOMAS, LANCE LEONARD BARRY, and STEPHEN C. SIU, *Administrative Patent Judges*.

SIU, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

This is a decision on appeal under 35 U.S.C. § 134(a) from the Examiner's rejection of claims 1-74 and 78-80. Claims 75-77 and 81 have been cancelled. We have jurisdiction under 35 U.S.C. § 6(b). An oral hearing was held on February 4, 2010.

The Invention

The disclosed invention relates generally to first principles simulation in semiconductor manufacturing processes (Spec. 1).

Independent claim 1 is illustrative:

> 1. A method of controlling a process performed by a semiconductor processing tool, comprising:
>
> inputting process data related to an actual process being performed by the semiconductor processing tool;
>
> inputting a first principles physical model including a set of computer-encoded differential equations, the first principles physical model describing at least one of a basic physical or chemical attribute of the semiconductor processing tool;
>
> performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed, said first principles simulation result being produced in a time frame shorter in time than the actual process being performed; and
>
> using the first principles simulation result obtained during the performance of the actual process to control the actual process performed by the semiconductor processing tool.

The References

The Examiner relies upon the following references as evidence in support of the rejections:

Chen	US 5,719,796	Feb. 17, 1998
Tan	US 6,263,255 B1	Jul. 17, 2001
Sonderman	US 6,802,045 B1	Oct. 05, 2004 (filed Apr. 19, 2001)
Nikoonahad	US 6,812,045 B1	Nov. 02, 2004 (filed Sep. 20, 2001)

Fatke US 2005/0016947 A1 Jan. 27, 2005
(filed Mar. 25, 2002)

V. K. Jain and A. D. Snyder, *Mathematic-Physical Engine: Parallel Processing for Modeling and Simulation of Physical Phenomena*, 1994 Int'l Symposium on Parallel Architectures, Algorithms and Networks (ISPAN), 366-373 (IEEE, 1994) ("Jain").

N. Yonemura, et al., *Heat Analysis on Insulated Metal Substrates*, 1996 Industry Applications Conference, Thirty-First IAS Annual Meeting, IAS '96, Vol 3, 1407-1410 (IEEE, 1996) ("Yonemura").

The Rejections

1. The Examiner rejects claims 1, 38, and 78 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain, and Tan.[1]
2. The Examiner rejects claims 1-21, 29, 30, 32-34, 37, 38-58, 66, 67, 69-71, 74, and 78-80 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman and Jain.
3. The Examiner rejects claims 22 and 59 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain, and Yonemura.

[1] The Examiner states in a paragraph heading that claims 1, 8, and 75 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain and Tan (Ans. 5). We note that claim 75 has been cancelled, claim 78 is similar to claim 1, and the Examiner discusses the rejection with regard to claims 1, 38, and 75 rather than claims 1, 8, and 75 (Ans. 5-7). Based on these observed discrepancies, we assume that the Examiner rejects claims 1, 38, and 78 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain, and Tan.

4. The Examiner rejects claims 23-28 and 60-65 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain, and Chen.
5. The Examiner rejects claims 31, 36, 68, and 73 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman, Jain, and Nikoonahad.
6. The Examiner rejects claims 35 and 72 under 35 U.S.C. § 103(a) as being unpatentable over Sonderman and Fatke.

ISSUE 1

The Examiner finds that the combination of Sonderman and Jain would have rendered claims 1, 38, and 78 obvious to one of ordinary skill in the art (Ans. 8-16).

Appellant disputes the Examiner's finding (App. Br. 26-27).

Did Appellant demonstrate that the Examiner erred in finding that claims 1, 38, and 78 would have been obvious to one of ordinary skill in the art based on the combination of Sonderman and Jain?

ISSUE 2

The Examiner finds that the combination of Sonderman, Jain, and Tan would have rendered claims 1, 38, and 78 obvious to one of ordinary skill in the art (Ans. 5-7).

Appellant disputes the Examiner's finding (App. Br. 16-26).

Did Appellant demonstrate that the Examiner erred in finding that the combination of Sonderman, Jain, and Tan discloses or suggests claims 1, 38, and 78?

FINDINGS OF FACT

The following Findings of Facts (FF) are shown by a preponderance of the evidence:

1. Sonderman discloses "a method and an apparatus for implementing a control simulation environment into a manufacturing environment" (Abstract).
2. Sonderman discloses a "process control environment 180, a manufacturing/processing environment 170, and a simulation environment 210" (col. 4, ll. 49-51).
3. Sonderman discloses that the "simulation environment 210 allows for testing various manufacturing factors in order to study and evaluate the interaction between the manufacturing factors" (col. 4, ll. 59-61).
4. Sonderman discloses that the "manufacturing environment 170 can send metrology data results into the simulation environment 210" and that the "simulation environment 210 can then use the metrology data results and perform various tests and calculations to provide . . . modified control parameters to the process control environment 180" (col. 5, ll. 1-6).

5. Sonderman discloses that the "process control environment 180 sends the modified or adjusted process control parameters to the manufacturing environment 170 for further processing of semiconductor wafers" (col. 5, ll. 7-10).
6. Tan discloses "semiconductor manufacturing process control" (col. 1, l. 12).
7. Tan discloses a need for a system that provides "[m]odel-based real-time process control using in situ inputs, process models, and process control strategies to correctly process control parameters during the process run" (col. 2, ll. 7-10).
8. Tan subsequently discloses a "set of cooperating components to address the above-mentioned problems" (col. 2, ll. 61-62).

PRINCIPLES OF LAW

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17-18 (1966).

"The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

ANALYSIS

Issue 1

Appellant argues that Sonderman fails to disclose or suggest "performing first principles simulation for the actual process being performed *during performance of the actual process*" or "the *first principles simulation result being produced in a time frame shorter in time than the actual process being performed*" (Reply Br. 9).

The Examiner finds that Sonderman discloses the disputed features (Ans. 23-24). As described above, Sonderman discloses simulation, process, and manufacturing environments (FF 1) in which the simulation and process environments produce process parameters that the manufacturing environment uses to perform processes (FF 2-3). The manufacturing environment may thus produce metrology data that may be returned to the simulation environment to produce updated process parameters for future processing of semiconductor wafers by the manufacturing environment (FF 4-5). Thus, Sonderman discloses a system in which a simulator (i.e., simulation environment) produces parameters for use in a manufacturing environment (i.e., an "actual process"). Since the manufacturing environment utilizes parameters generated by the simulation environment, the simulation environment must complete processing prior to the performance of the actual process by the manufacturing environment such that the manufacturing environment may utilize the parameters generated by the simulation environment. Therefore, we cannot agree with the Examiner

that Sonderman discloses that the simulation is performed during the performance of the actual process, as recited in claim 1.

The Examiner finds that Sonderman discloses performing a simulation during performance of the actual process because Sonderman discloses that "target values are then used to generate new control inputs, X_{Ti} on line 805 to control a subsequent process of a silicon wafer S_i" (Ans. 24; Sonderman, col. 9, ll. 44-46). However, Sonderman discloses applying values to a *subsequent* process. We interpret the term "subsequent" to indicate a process that follows a prior (or current) process. Since the values generated in Sonderman are generated for a subsequent process (i.e., a process to be performed in the future) rather than generating parameters for a process that is currently being performed, we cannot agree with the Examiner's finding.

Claims 38 and 78 recite similar features as claim 1. Also, the Examiner does not find that Jain, Yonemura, Chen, Nikoonahad, or Fatke disclose or suggest the disputed feature discussed above.

Accordingly, we conclude that Appellant has shown that the Examiner erred in rejecting independent claims 1, 38, and 78 under 35 U.S.C. 103(a), and of claims 2-37, 39-74, 79, and 80, which depend therefrom.

Issue 2

As described above, Sonderman discloses processing parameters in a simulation environment for a manufacturing process. Tan discloses a system that solves the problem of processing parameters for a process (i.e., a manufacturing process) "during the process run" (FF 6-8). Since Tan discloses addressing the problem of processing parameters in a simulation of

a process "during the process run," we agree with the Examiner that the combination of Sonderman, Jain, and Tan discloses or suggests performing a simulation during performance of the actual process.

Appellant argues that Tan discloses using "post-process data to update a model for a subsequent process step" (App. Br. 20). However, we cannot agree with Appellant that Tan only discloses generating data for a subsequent process step in view of Tan's explicit disclosure of "address[ing] the above-mentioned problems" (col. 2, l. 62) of processing "control parameters during the process run" (col. 2, ll. 9-10).

Appellant also argues that "the combination [of Sonderman, Jain, and Tan] would not disclose or suggest that a simulation result is produced in a time frame shorter in time than the actual process being performed, as claimed" (App. Br. 20-21). However, if process parameters for an actual process are being generated during the performance of the actual process, as disclosed by Tan, then it would have been obvious to one of ordinary skill in the art that the simulation would be completed earlier in time than the actual manufacturing process since the actual manufacturing process would need the parameters generated by the simulation to be executed and would therefore complete after the simulation.

We agree with the Examiner that it would have been obvious to one of ordinary skill in the art, given that a simulation generates parameters to be used in a manufacturing process that is being performed simultaneously with the simulation, that the simulation would generate the parameters and thus be completed prior to the completion of the manufacturing process. In such

a scenario, the time frame of the simulation would be shorter than that of the manufacturing process since if the time frame of the simulation was longer than the manufacturing process, the simulation would not have generated the parameters needed by the manufacturing process prior to completion of the manufacturing process (which cannot be complete since the manufacturing process has not yet obtained the needed parameters from the simulator).

For at least the aforementioned reasons, we conclude that Appellant has not sustained the requisite burden on appeal in providing arguments or evidence persuasive of error in the Examiner's rejection of claims 1, 38, and 78 with respect to issue 2.

CONCLUSION OF LAW

Based on the findings of facts and analysis above, we conclude that Appellant has demonstrated that the Examiner erred in finding that claims 1, 38, and 78 would have been obvious to one of ordinary skill in the art based on the combination of Sonderman and Jain (issue 1) but has failed to demonstrate that the Examiner erred in finding that claims 1, 38, and 78 would have been obvious to one of ordinary skill in the art based on the combination of Sonderman, Jain, and Tan (issue 2).

DECISION

We affirm the Examiner's decision rejecting claims 1, 38, and 78 as obvious under 35 U.S.C. § 103 over Sonderman, Jain, and Tan. We reverse the Examiner's decision rejecting claims 1-74 and 78-80 as being obvious

under 35 U.S.C. § 103 over Sonderman and Jain in view of either Yonemura, Chen, Nikoonahad, or Fatke.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

msc

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